

# BINARY NUMBERS

Binary numbers contain only 0's and 1's.

Ex:  $(110101)_2 = 2^0 + 2^2 + 2^4 + 2^5 = 1 + 4 + 16 + 32 = (53)_{10}$

↑ base  
↘  
conversion

Summation and Subtraction:

$$\begin{array}{r} 101101 \\ + 100111 \\ \hline 1010100 \end{array}$$

$$\begin{array}{r} 101101 \\ - 100111 \\ \hline 000110 \end{array}$$

Product:

$$\begin{array}{r} 1011 \\ \times 101 \\ \hline 1011 \\ 0000 \\ + 1011 \\ \hline 110111 \end{array}$$

Complements: are used to show negative binary.

1's complement:

1's comp:

$$1011000 \longrightarrow 0100111$$

2's comp: Add 1 to 1's complement.

Ex:  $11011000 \xrightarrow{2's\ comp.} 00100111$

$$\begin{array}{r} 00100111 \\ + 1 \\ \hline 00101000 \end{array}$$

## Subtraction with Complements:

The subtraction of two numbers  $M-N$

- 1) Add  $M$  to the 2's comp of  $N$ .
- 2) If  $M \geq N$ , the sum produces an end carry which is discarded.
- 3) If  $M < N$ , the sum does not produce a carry.  
To obtain the answer, take the 2's complement of the sum and place a negative in front.

Ex: Given

$$X = 1010100 \text{ and}$$

$$Y = 1000011, \text{ perform the subtraction}$$

- a)  $X - Y = ?$       b)  $Y - X = ?$  by using 2's complement

a)  $X = 1010100$

2's comp of  $Y = 0111101$

$$\begin{array}{r} 1010100 \\ + 0111101 \\ \hline 10010001 \end{array}$$

end carry →      ↑ discard

answer = 0010001

b)  $Y = 1000011$

2's comp of  $X = 0101100$

$$\begin{array}{r} 0101100 \\ + 1011111 \\ \hline 1101111 \end{array}$$

if it is 1  
it is negative

therefore the answer is  $Y - X = - (2's \text{ comp of } 1101111)$   
OR  
 $= -0010001$

x(-)

# Binary Logic

AND op:

Binary variable X and Y.

X.Y means X AND Y.

X	Y	X.Y
0	0	0
1	1	1
0	1	0
1	0	0

↑ truth table

OR op:

X	Y	X+Y
1	0	1
0	1	1
1	1	1
0	0	0

NOT op:

X	X' = $\bar{X}$
0	1
1	0

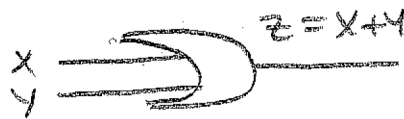
# Logic Gates

Logic gates are electronic circuits that operate with inputs to produce an output.

AND:



OR:



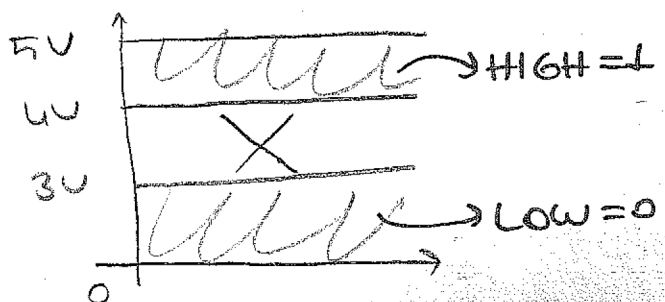
NOT:



Voltage = electrical energy

0V → 0

5V → 1



# Boolean Algebra and Logic Gates

## Binary Algebra

### Theorems:

$$X + 0 = X$$

$$X + X' = 1$$

$$X + X = X$$

$$X + 1 = 1$$

$$(X')' = X$$

$$X + Y = Y + X$$

$$X + (Y + Z) = (X + Y) + Z$$

$$X(Y + Z) = XY + XZ$$

$$(X + Y)' = X'Y'$$

$$X + XY = X$$

$$X \cdot 1 = X$$

$$X \cdot X' = 0$$

$$X \cdot X = X$$

$$X \cdot 0 = 0$$

$$XY = YX$$

$$X(YZ) = (XY)Z$$

$$X + YZ = (X + Y)(X + Z)$$

$$(XY)' = X' + Y'$$

$$X(X + Y) = X$$

### Operator Precedence:

Paranthesis  $\rightarrow$  NOT  $\rightarrow$  AND  $\rightarrow$  OR

### Boolean functions:

$F_1 = X + Y'Z$   
 function      Input variables: X, Y, Z

### Truth Table

X	Y	Z	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1



## Algebraic Manipulations:

Ex: Simplify the problem functions.

$$1- x(x' + y) = \underbrace{x \cdot x'}_0 + xy = xy$$

$$2- x + x'y = \underbrace{(x + x')}_1 (x + y) = x + y$$

$$3- (x + y)(x + y') = xx + xy' + x'y \oplus yy' \xrightarrow{0}$$
$$x(1 + \underbrace{y' + y})_1 = x$$

$$4- xy + x'z + yz = xy + x'z + yz(x + x')$$
$$= xy + x'z + xy'z + x'y'z$$
$$= xy(1 + z) + x'z(1 + y) = xy + x'z$$

## Complement of a Function

De Morgan's Theorem:

$$(A + B + C + \dots + F)' = A' B' C' \dots F'$$

$$(ABCD \dots F)' = A' + B' + C' + \dots + F'$$

Ex: Find the complement of the function

$$F_1 = x'y'z' + x'y'z \quad \text{and} \quad F_2 = x(y'z' + yz)$$

$$F_1' = (x'y'z' + x'y'z)' = (x'y'z')' (x'y'z)'$$
$$= (x + y' + z)(x + y + z')$$

$$F_2' = [x(y'z' + yz)]' = x' + (y'z' + yz)'$$
$$= (x' + (y'z')')(yz)' = x' + yz' + y'z$$

## Minterms and Maxterms

Given;

X	Y	Z	minterm	maxterm
0	0	0	$X'Y'Z' \rightarrow m_0$	$X+Y+Z \rightarrow M_0$
0	0	1	$X'Y'Z \rightarrow m_1$	$X+Y+Z' \rightarrow M_1$
0	1	0	$X'YZ'$	$X+Y'+Z$
0	1	1	$X'YZ$	$X+Y'+Z'$
1	0	0	$XY'Z'$	$X'+Y+Z$
1	0	1	$XY'Z$	$X'+Y+Z'$
1	1	0	$XYZ'$	$X'+Y'+Z$
1	1	1	$XYZ$	$X'+Y'+Z'$

Suppose a function

$$f_1 = X'Y'Z + XY'Z' + XYZ$$

$$= m_1 + m_4 + m_7$$

If

$$f_1' = X'Y'Z + X'YZ' + X'YZ + XY'Z' + XYZ'$$

$$= m_0 + m_2 + m_3 + m_5 + m_6 \quad (\text{sum of min terms})$$

If

$$(f_1')' = (X+Y+Z)(X+Y'+Z)(X'+Y+Z')(X'+Y'+Z)(X+Y+Z')$$

$$= M_0 \cdot M_2 \cdot M_3 \cdot M_5 \cdot M_6$$

(product of max terms)

$$= f_1$$

Thus;

Any function  $f$  can be shown as SOP or POS form.

EX:  $f_1 = \sum (1, 4, 7)$  (SOP)

or

$f_2 = \prod (0, 2, 3, 5, 6)$  (POS)

conversion;

$$\boxed{m_j' = M_j}$$

Standard forms: (SOP), (POS)

EX: In SOP form

$$f_1 = y' + xy + x'y'z'$$

find the minterms:

$$f_1 = y' ( \underbrace{xz + x'z + xz' + x'z'}_{\substack{z(x+x') + z'(x+x') \\ \downarrow \quad \downarrow \\ z+z' \\ \downarrow}} ) + xy(z+z') + x'y'z'$$

OR

$$= \underbrace{xy'z}_{m_5} + \underbrace{x'y'z}_{m_1} + \underbrace{xy'z'}_{m_4} + \underbrace{x'y'z'}_{m_0} + \underbrace{xyz}_{m_3} + \underbrace{xy'z'}_{m_6} + \cancel{\underbrace{x'y'z'}_{m_7}}$$

$$f_1 = \sum (0, 1, 4, 5, 6, 7)$$

## EXCLUSIVE OR

$$X+Y = XY' + X'Y$$

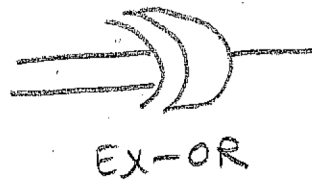
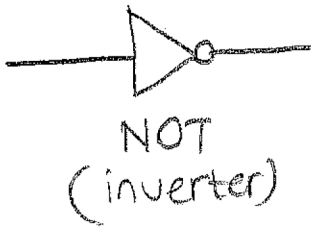
NOR

$$(X+Y)'$$

NAND

$$(X \cdot Y)'$$

## Logic Gates



# Gate Level Minimization

## The map method

K-map: Karnaugh Map

2-variable K-map:

$m_0$	$m_1$
$m_2$	$m_3$

Inputs: X and Y

	0	1
0	$m_0$	$m_1$
1	$m_2$	$m_3$

Ex: simplify the following function by K-map.

$$f = X'Y + XY' + XY = X + Y = \sum (1, 2, 3)$$

f =

	0	1
0	0	1
1	1	1

### Grouping

1. Adjacent cells
2. Power of 2.  $2^n$ ,  $n = \#$  of groups
3. Large groups

$f = X + Y$
-------------

↓  
minterm addition (+)

### 3-Variable K-map:

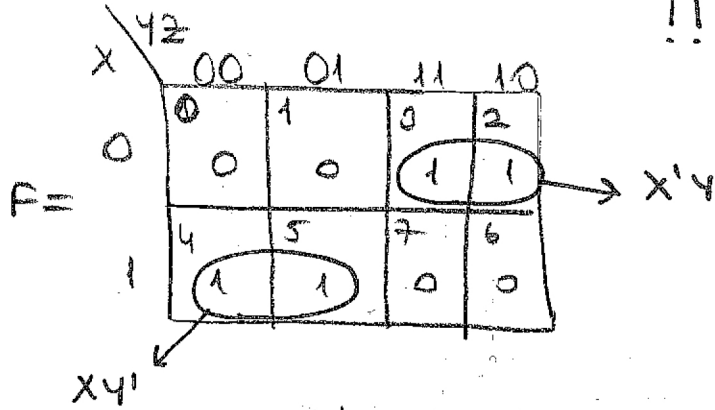
→ minterm

Ex:  $F(x, y, z) = \sum (3, 4, 5)$

simplify by K-map

Solution:

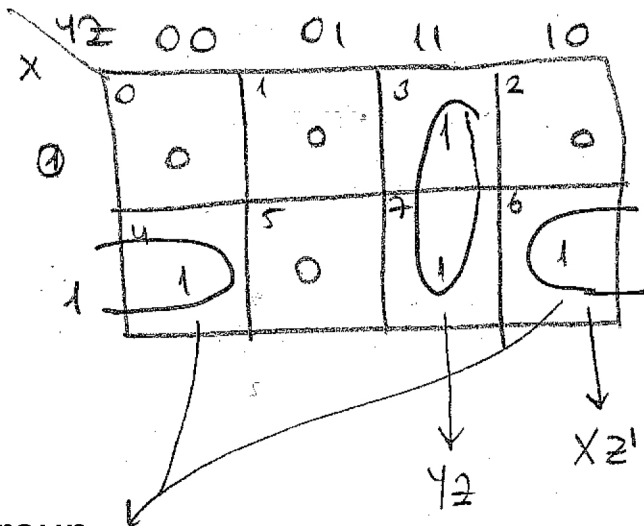
(at the given minterm you put 1.)  
!!!!!!



$= x'y + xy' = x \oplus y$

Ex:  $F(x, y, z) = \sum (3, 4, 6, 7)$

simplify by K-map.



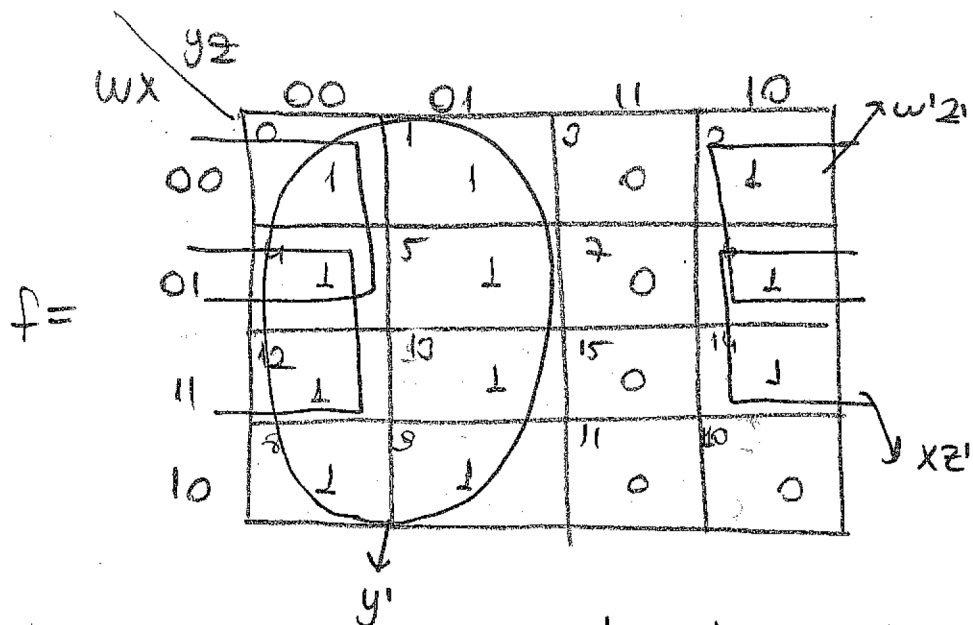
$= xz' + yz$

Group

### 4-Variable K-map:

Ex:  $F(w, x, y, z) = \sum (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$

Simplify by K-map.

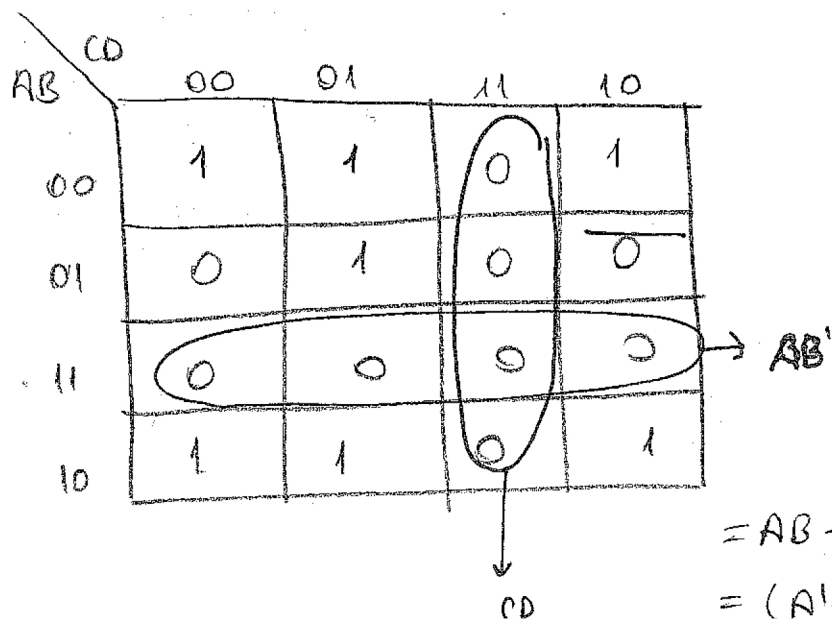


$$f = y' + w'z' + xz'$$

Ex: Simplify

$$F(A, B, C, D) = \sum (0, 1, 2, 5, 8, 9, 10)$$

max-term in K-map



$$= AB + CD + BD'$$

$$= (A+B)(C+D)(B'+D)$$

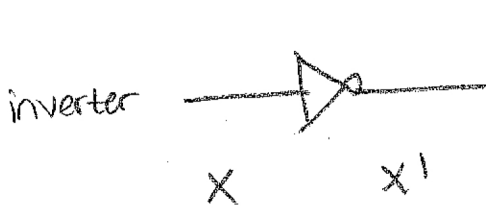
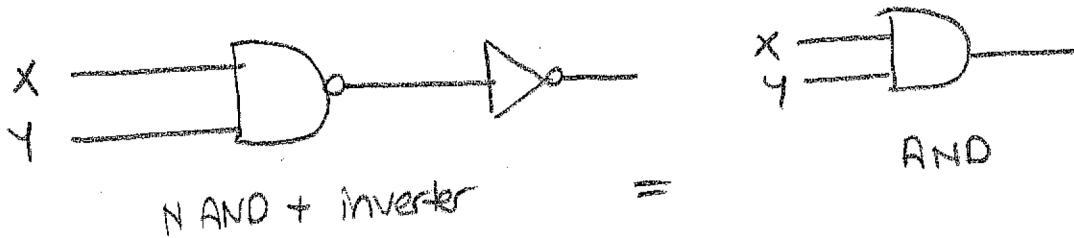
# DON'T CARE

If the function value does not matter then we use don't care (x)

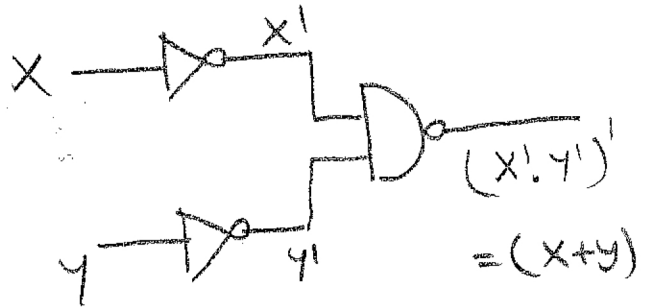
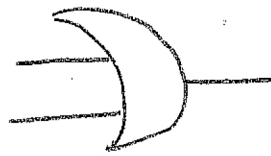
don't care can be grouped as you wish.

## NAND Implementation

Circuits:



OR

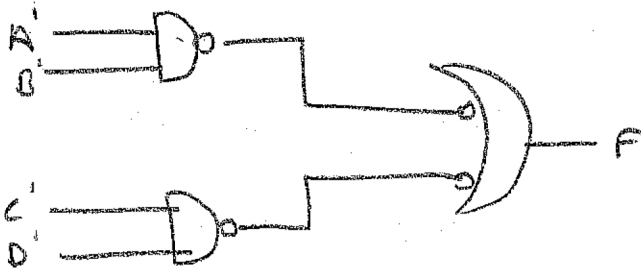
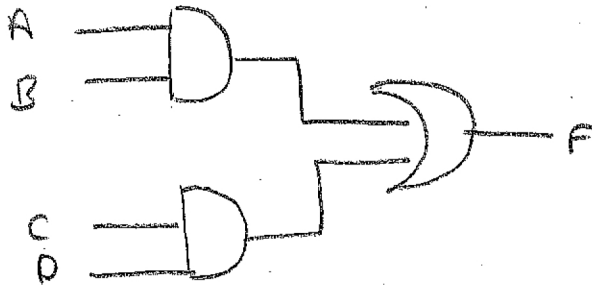




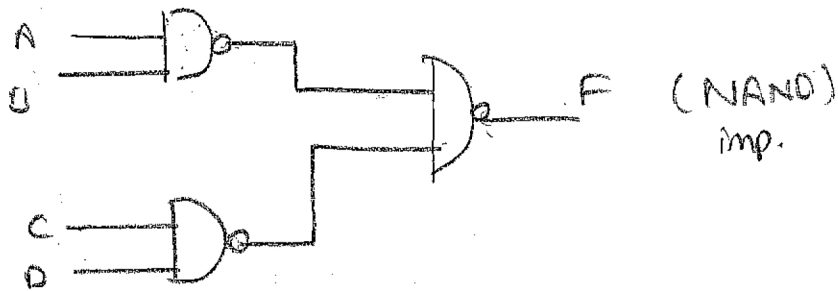
Ex: Implement the following function using NAND logic

$$F = AB + CD$$

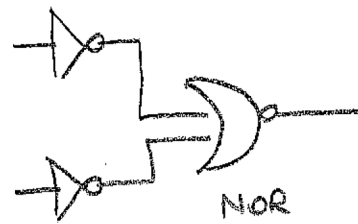
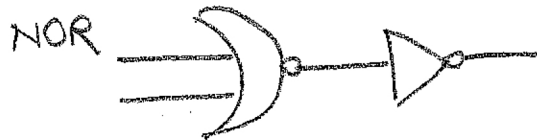
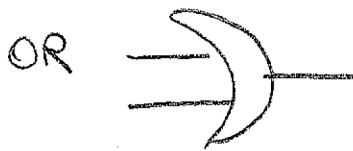
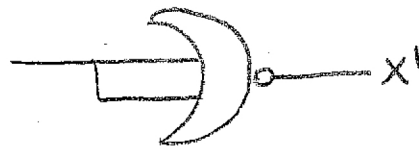
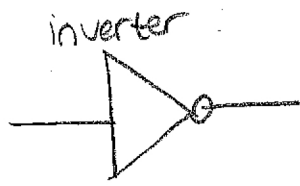
$$F = [(AB)'] \cdot [(CD)']' = [(A'B)'] \cdot [(C'D)']$$



||



# NOR implementation



Exclusive OR function:

$$X \oplus y = xy + x'y$$

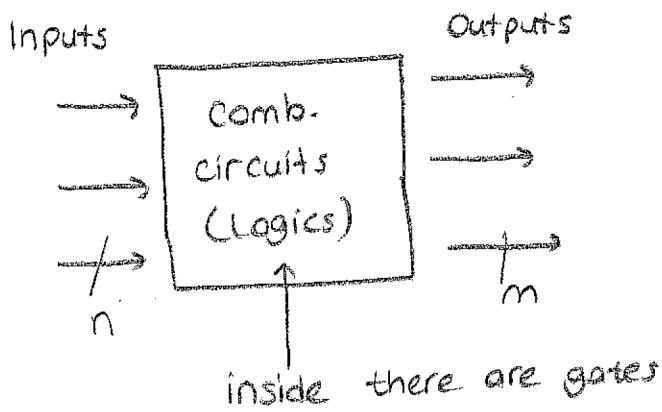
X	y	X+y
0	0	0
0	1	1
1	0	1
1	1	0

X	y	z	X+y+z
0	0	0	0
0	0	1	1
0	1	0	1
1	0	0	1
0	1	1	0
1	1	0	0
1	1	1	1
1	0	1	0

rule = even numbers = 0

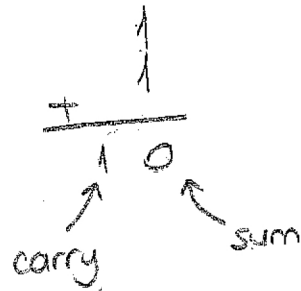
# Combinational Logic

Consists of inputs, gates and outputs.



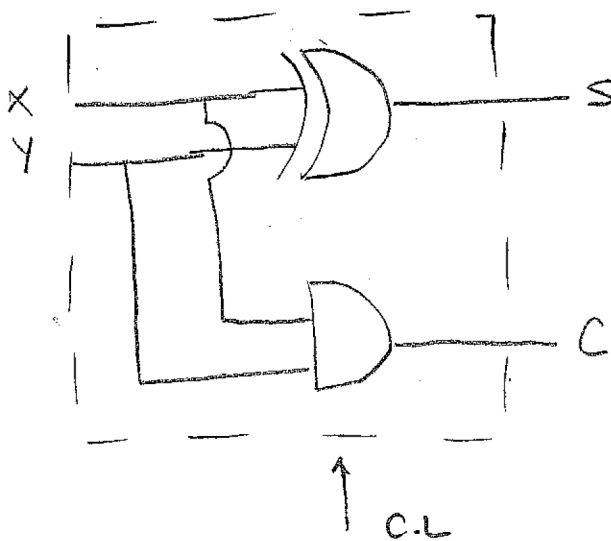
Half-Adder: (1 bit binary adder)

X	Y	Carry C	Sum S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



$$S = X \oplus Y \text{ OR}$$

$$C = X \odot Y \text{ AND}$$



### Full-Adder:

Add 3 1-bit binary number.

①

X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

### ② Simplification:

S =

X \ YZ	00	01	11	10
0	0	1	0	1
1	1	0	1	0

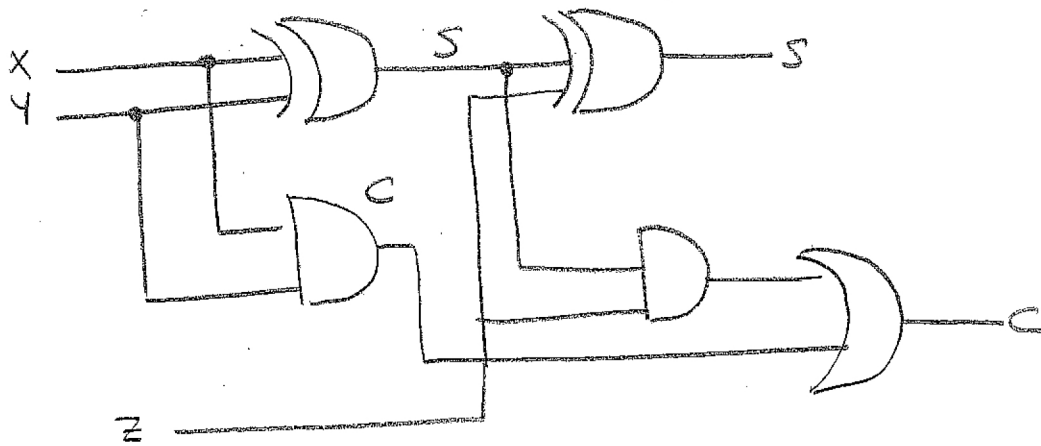
$$= X'Y'Z + X'YZ' + XY'Z' + XYZ$$

C =

X \ YZ	00	01	11	10
0			1	
1		1	1	1

$\downarrow$     $\downarrow$     $\downarrow$   
 XZ   YZ   XY

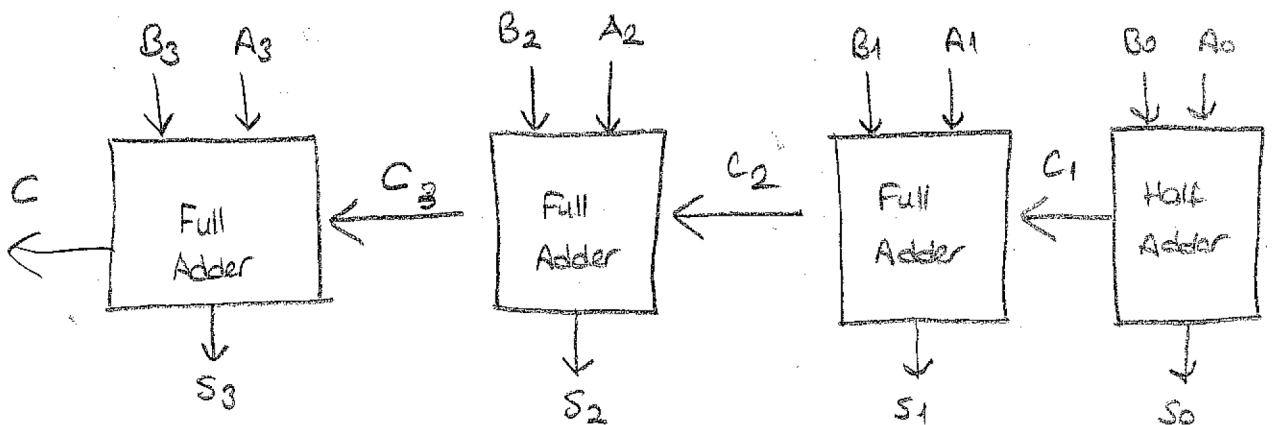
$$= XZ + YZ + XY$$



$$\begin{array}{r}
 X \\
 + Y \\
 \hline
 CS \\
 + Z \\
 \hline
 \end{array}$$

Addition of 2 4-bit Binary Numbers:

$$\begin{array}{r}
 C \quad C \quad C \\
 A_3 \quad A_2 \quad A_1 \quad A_0 \\
 + B_3 \quad B_2 \quad B_1 \quad B_0 \\
 \hline
 C \quad S_3 \quad S_2 \quad S_1 \quad S_0 \\
 \underbrace{\hspace{10em}}_{\text{full adder}} \quad \underbrace{\hspace{5em}}_{\text{half adder}}
 \end{array}$$



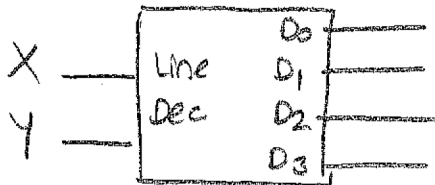
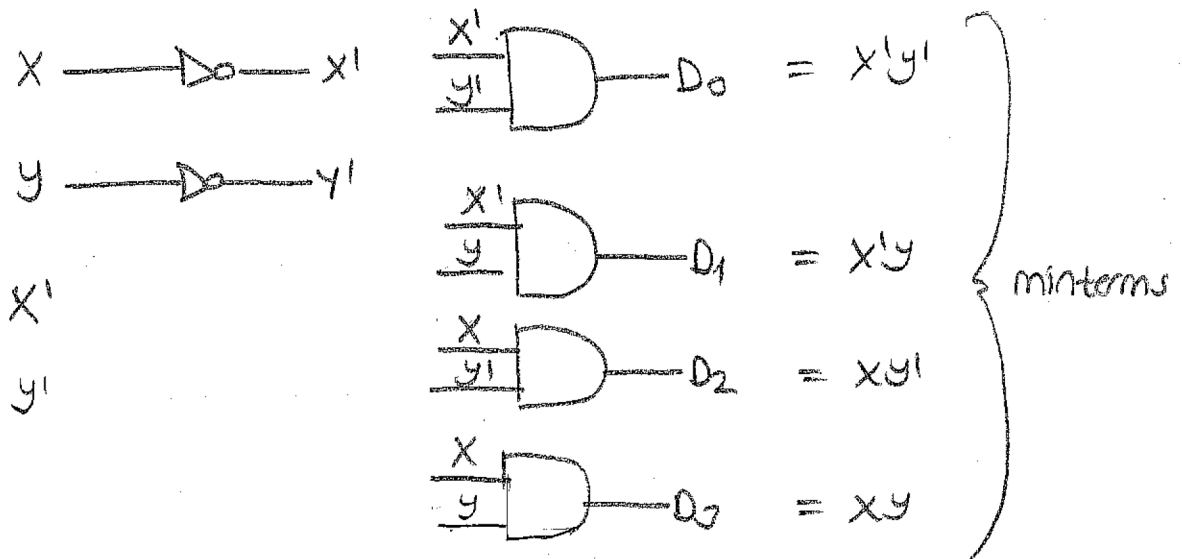


EX: Line-Decoders

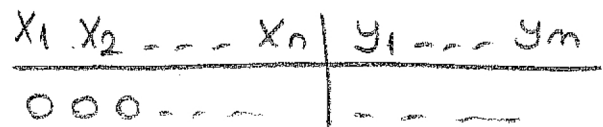
Generate minterms

Given 2 inputs design a line-decoder

Ans:



C.L Implementation by Decoders:



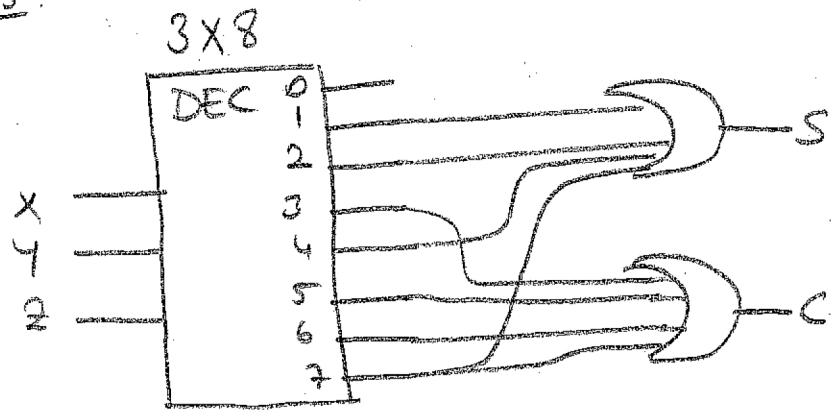
EX: Implement the C.L for

$$S(X, Y, Z) = \sum (1, 2, 4, 7)$$

$$C(X, Y, Z) = \sum (3, 5, 6, 7)$$

by using a line-decoder

Ans:



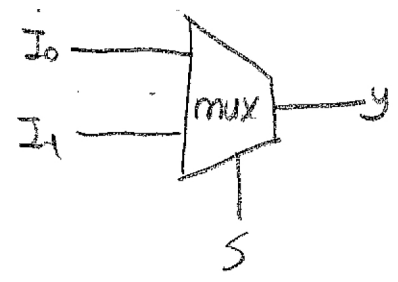
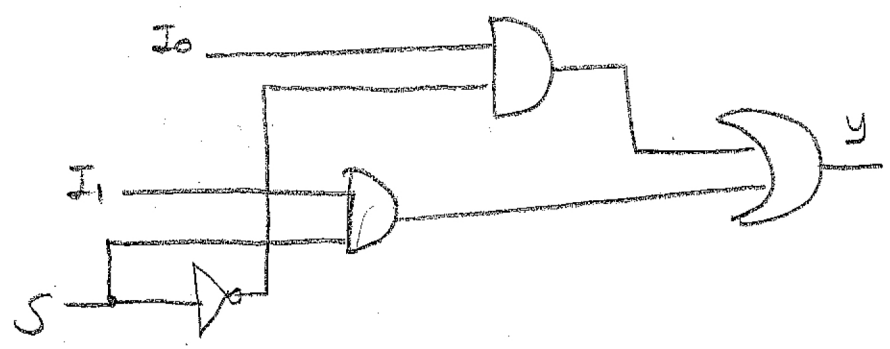
**ENCODER:**

It's the opposite of decoder

**Multiplexer (mux):**

It's a C.L. circuit that selects one of many inputs into a single output

EX: 1x1 mux



S	y
0	I <sub>0</sub>
1	I <sub>1</sub>

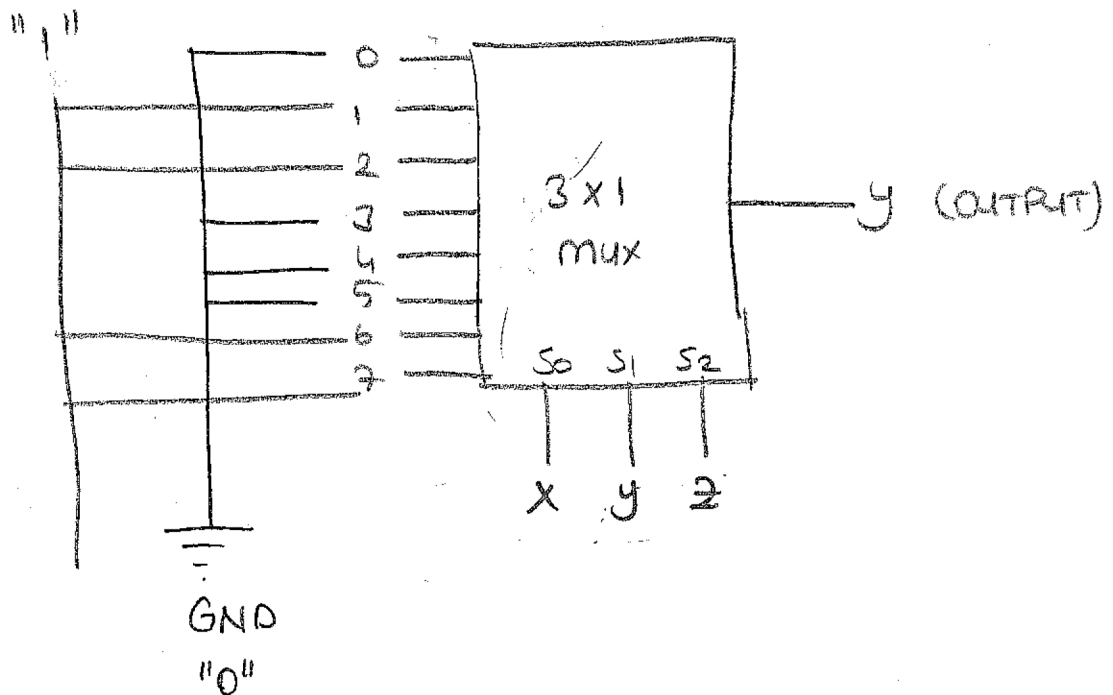


# Boolean function Implementation

EX: (3) x (1) mux  
selective output

implement

$F(x, y, z) = \sum (1, 2, 6, 7)$  by using a multiplexer



## NAND Implementation:

EX:

$$f_1 = AB' + A'C + A'BC'$$

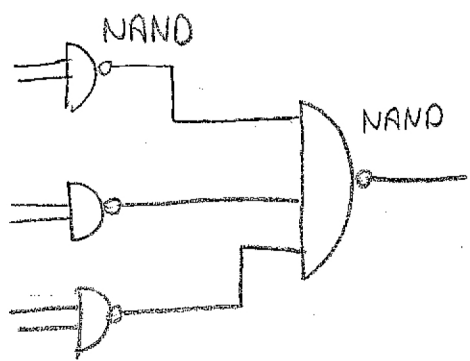
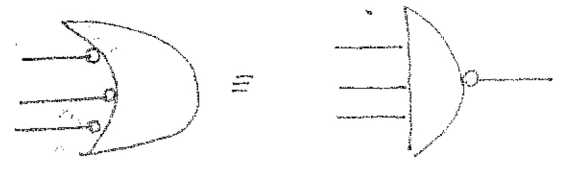
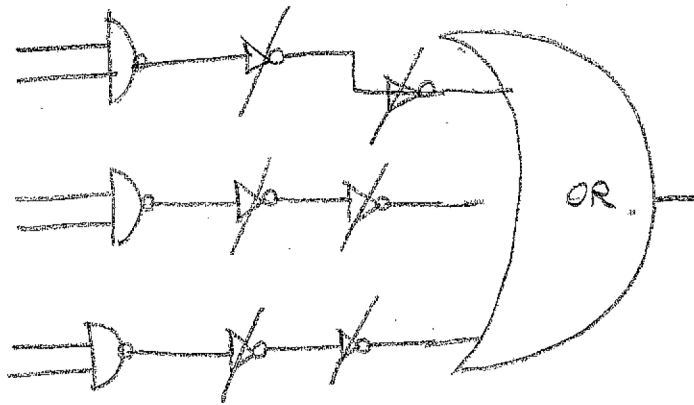
$$= AB' + A'(C + BC')$$

$$= (C+B)(C+C')$$

$$= AB' + A'C + A'B = [(AB')' \cdot (A'C)' \cdot (A'B)']'$$

(SOP)

if in sop form: then replace all the gates by the NAND gate.

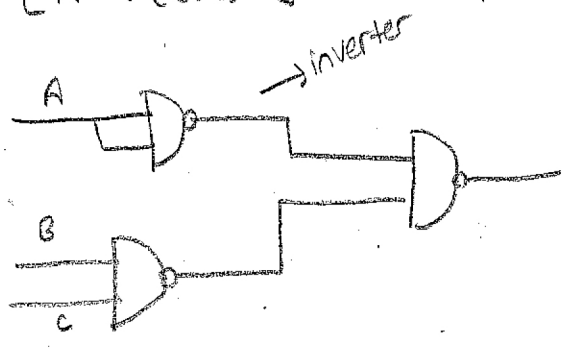


$$f_2 = A + BC$$

$$= A \cdot A + B \cdot C$$

$$= [(A \cdot A)' \cdot (B \cdot C)']'$$

$$= [A' \cdot (B \cdot C)']'$$



$$f_3 = (A' + C)(A + B') \quad (\text{POS form})$$

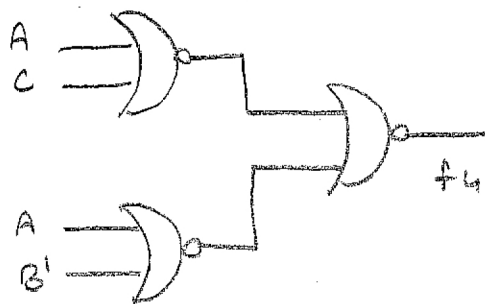
$$= \cancel{A}A' + A'B' + CA + CB'$$

= Then proceed as usual.

NOR implementation:

$$f_4 = (A + C) \cdot (A + B') \quad (\text{POS})$$

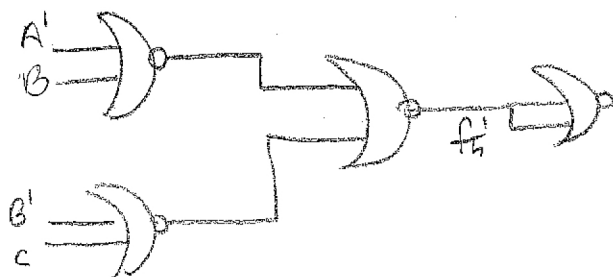
$$f_4 = [(A + C)' + (A + B')']'$$



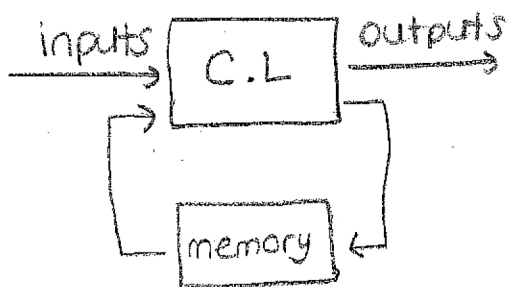
$$f_5' = [AB' + BC']'$$

$$= (AB')' \cdot (BC')' = (A' + B)(B' + C) \quad (\text{POS})$$

$$f_5' = [ [(A' + B)' + (B' + C)'] ]' \quad \swarrow \text{last inv.}$$



# \_ Sequential Logic \_



sequential circuits contain memory.

Two type of sequential circuits

Synchronous

All outputs are generated at the same time determined by a "clock signal".

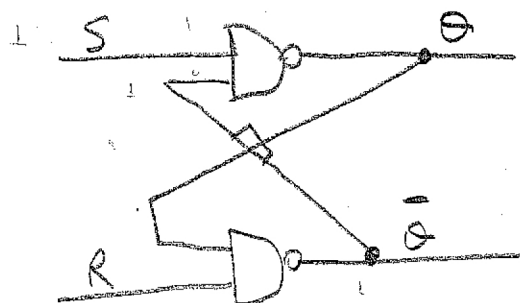
Async

Not all outputs are generated at the same time

The storage element (memory) is flip-flop.

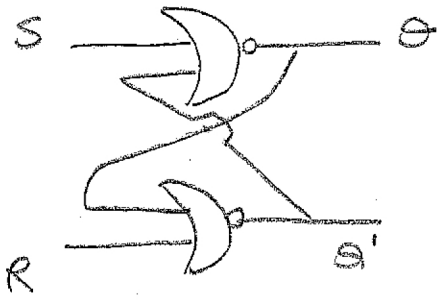
Latches: (First form of flip-flop)

SR Latch.



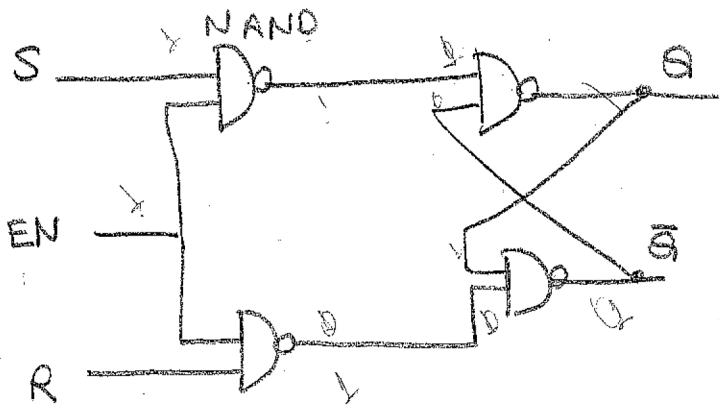
S	R	Q	$\bar{Q}$
1	0	0	1 (Set)
1	1	0	1 (Latch)
0	1	1	0 (Reset)
1	1	1	0 (Latch)
0	0	1	1 (forbidden)

## SR-NOR-Latch:



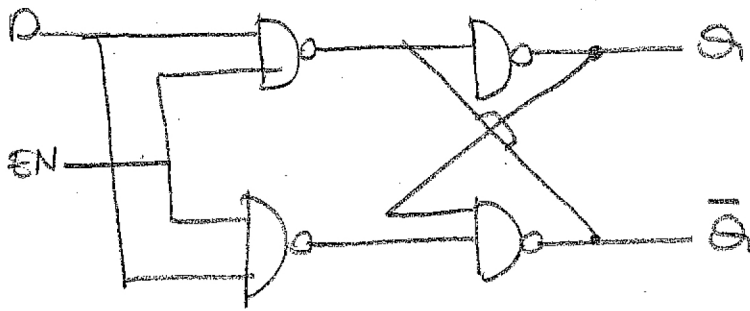
S	R	Q	Q'	
1	0	1	0	(Set)
0	0	1	0	(Latch)
0	1	0	1	(Reset)
0	0	0	1	(Latch)
1	1	0	0	forbidden

## SR-Latch with Enable:



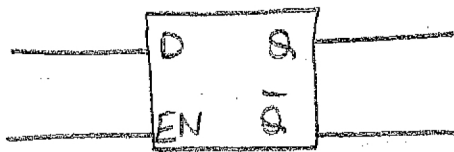
EN	S	R	Q	Q'
0	X	X	No change (eski degeri tutar)	
1	0	0	No change	
1	0	1	Q = 0 (Reset)	
1	1	0	Q = 1 (Set)	
1	1	1	Indetermined	

# D-Latch



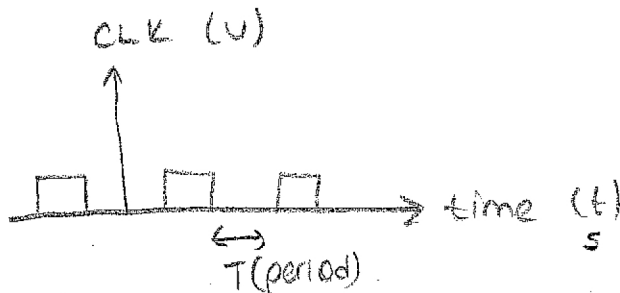
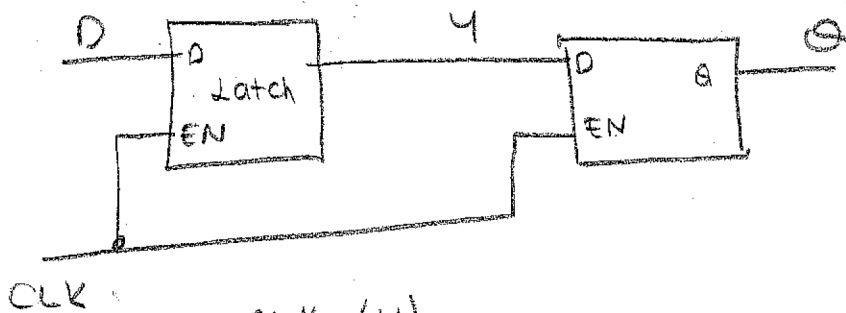
EN	D	Q
0	X	No change
1	0	0 (Reset)
1	1	1 (Set)

## Circuit Symbol for D-Latch:



Circuit Symbol

## D-Flip-Flop:

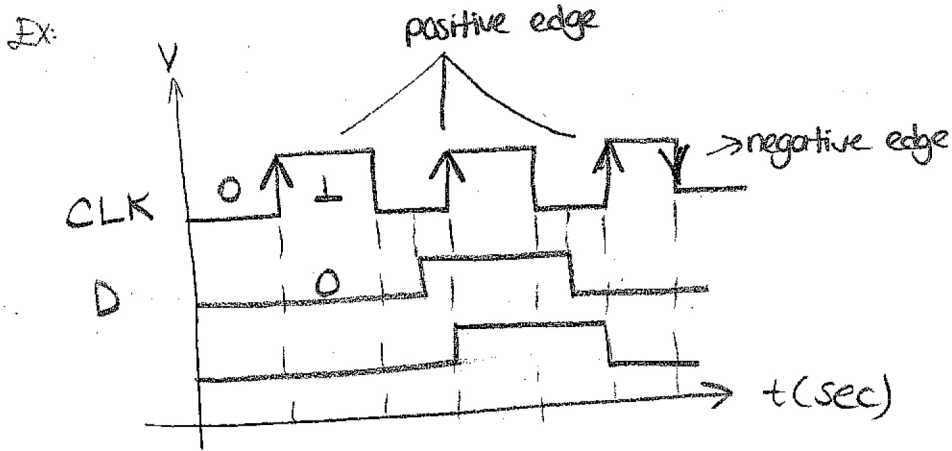
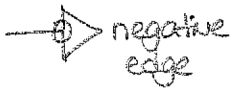
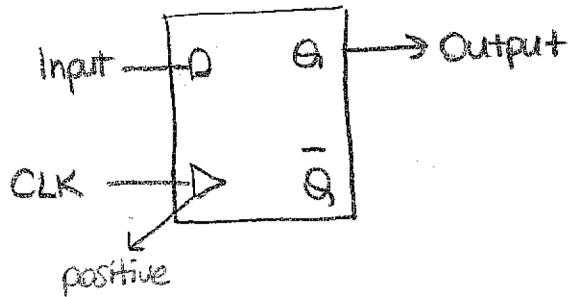


$$\frac{1}{T} = \text{frequency (Hz)}$$

$10^3$ - kilo (k)	$10^{-3}$ - milli (m)
$10^6$ - mega (M)	$10^{-6}$ - micro ( $\mu$ )
$10^9$ - giga (G)	$10^{-9}$ - nano (n)
$10^{12}$ - Tera (T)	$10^{-12}$ - pico (p)

## Edge Triggered D-FF:

D-Flip flop

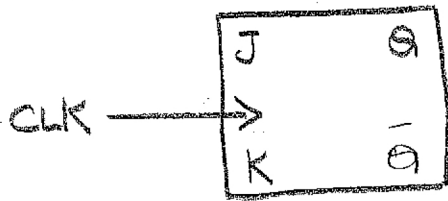


Draw the output (Q) wave to;

D	Q
0	0
1	1

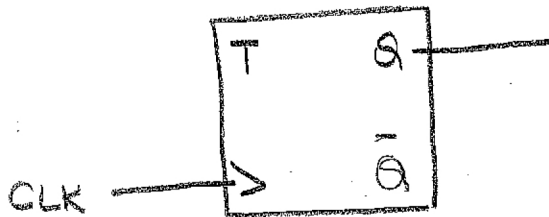
( $\uparrow$ )  $\rightarrow$  only at the raising edge (POS. EDGE)  
 ( $\downarrow$ )  $\rightarrow$  (NEG. EDGE)

# J-K Flip-Flop:



J	K	next value $Q(t+1)$	
0	0	$Q(t)$ means previous value	NO CHANGE
0	1	0	RESET
1	0	1	SET
1	1	$\bar{Q}(t)$	COMPLEMENT

# T-FF: (Toggle)



T	$Q(t+1)$	
0	$Q(t)$	NO CHANGE
1	$\bar{Q}(t)$	COMPLEMENT

## - Characteristic Equations -

for D-FF:  
 $Q(t+1) = D$

for J-K:  
 $Q(t+1) = JQ' + K'Q$

for T-FF:  
 $Q(t+1) = T \oplus Q$   
 $= TQ' + T'Q$

Ex: Draw the output wave form given.  
 (t edge D-FF)

