ECE 124 – Lab 1

Preparation

1) Study AND, OR and NOT gates, draw truth tables.
2) What is commutative, distributive and associative laws in Boolean algebra; explain each of them briefly with expressions.
3) What is DeMorgan law for Boolean algebra, explain briefly.

Experiment

1) Test truth tables for AND, OR and NOT gates, in your board by using 7408, 7432 and 7404.
2) Construct 4 AND gates together and test them by using 7408.
3) Construct 4 OR gates together and test them by using 7432.
4) Construct 3 NOT gates together and test them by using 7404.
5) By using 7404 and 7408, first take the inverse of two inputs and then use them for AND operation.

ECE 124 – Lab 2

PREPARATION:

1) Demonstrate by means of truth tables the validity of the following identities:
a) DeMorgan's theorem for three variables: (xyz)' = x' + y' + z'
b) The second distributive law: x + yz = (x + y)(x + z)

2) Simplify the following Boolean expressions to a minimum number of literals.
a) a'b' + ab + a'b
b) (a+b)(a+b')
c) a'b+ab'+ab+a'b'
d) a'+ac'+ab'c'
e) ab'+b'c'+a'c'

3) Simplify the following Boolean expressions to a minimum number of literals.
a) ABC+A'B+ABC'
b) X'yz+xz
c) (x+y)'(x'+y')
d) xy+x(wz+wz')
e) (BC'+A'D)(AB'+CD')

EXPERIMENT:
Set up 1-b, 2-a, 3-a.

ECE 124 LAB 3

1-) Simplify and Implement the following functions with NAND Gates.

a) a’b’ + ab + a’b
b) (a+b)(a+b’)

ECE 124 LAB 4

1-) Introduction to ORCAD Design Suite:

Following function is given.

$F_1(A,B,C) = AC + A'B+AB'C$

Construct the circuit in ORCAD.

ECE 124 LAB 5

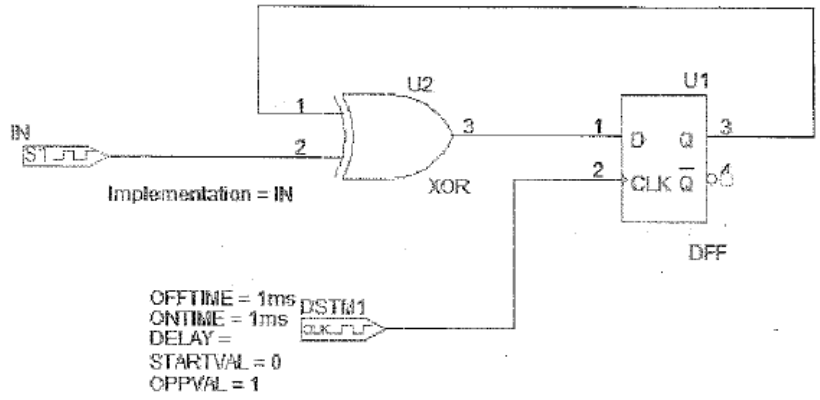
1. Design four bit adder. Operation: Assume that you have two 4-bit number and you have to add them and show the results on PSpice.
Hint: *Use half adders and full adders as combinational blocks.*

ECE 124 LAB 6

1-) Odd Parity Checker Circuit:

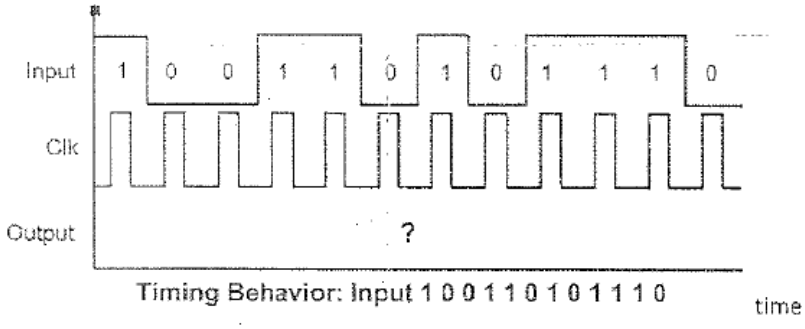
It outputs whenever input bit stream has odd # of 1's.

Implement the following circuit in OrCad. Show the results (output) to your instructor.



Parts – Libraries: DFF- digprim, XOR – digprim, digclock (DSTM1)– source, Digstim1 (IN)- sourcstm.

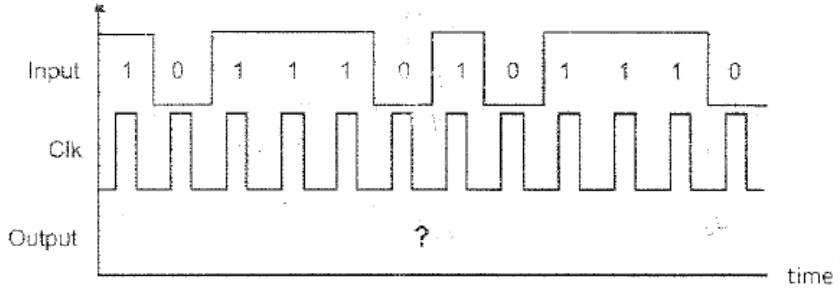
The use of Digital Stimulus will be explained in the lab.



Timing Behavior: Input 1 0 0 1 1 0 1 0 1 1 1 0

2-) Problem:

Design an fsm such that it outputs when three consequtive 1's are detected at the input bit stream. Draw the circuit and use the following input data. Show the results to your instructor.



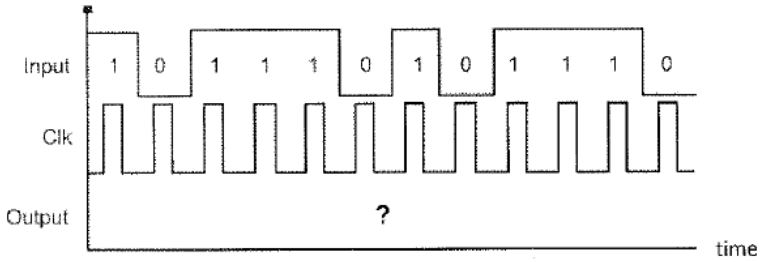
ECE 124 LAB 6(cont.)

1-) 011 Checker Circuit:

Design an fsm such that it outputs whenever input bit stream has 011.

Parts – Libraries: DFF- digprim, XOR – digprim, digclock (DSTM1)– source, Digstim1 (IN)- sourcstm.

Use the following test signal as the input.



Show your paper work and computer simulation circuit to your instructor.

ECE 124 LAB 7

1-) Counters:

a-) Design a 3 bit ripple up-counter out of TFF's.

b-) Design a 3 bit synchronous up-counter.

c-) Design a 3 bit counter that counts to decimal 5.

Ex: 000, 001, 010, 011, 100, 101, 000, …

Hint: Parts- Libraries: DFF,TFF- digprim, All gates – digprim, digclock(DSTM1)- source.

ECE 124 LAB 8

1) Designing 4x4 ROM

Design a 4x4 ROM
Store the following data into the memory.
1011,1010,1101,1001.

ECE 124 LAB 9

1) Designing 4x4 RAM

Design a 4x4 RAM. Store the following data into the memory.
1011,1010,1101,1001.
Read existing data and rewrite new values. Explain differences between RAM and ROM.

ECE 124 LAB 10

1-) Basic PLA(Programmable Logic Array) Implementation:

Two combinational logic function given below.

$F_1(A,B,C) = AC + A'B+AB'C$

$F_2(A,B,C) = [AC + B'C']'$

Construct these logic circuits by using PLA in ORCAD Design Suite and Simulate. Use "Digclock" for inputs(A,B,C). A sample PLA structure is given below in Figure-1.

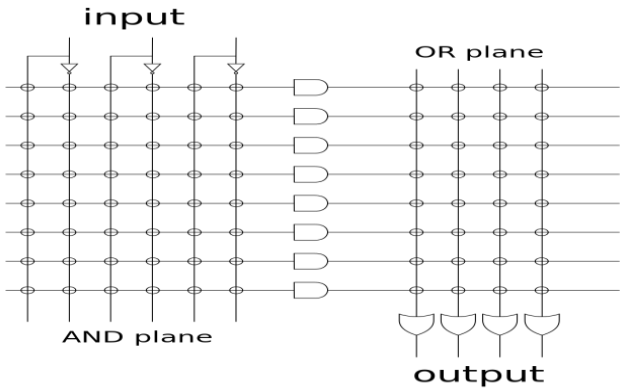


Figure-1[1]

2-) SPLD (Simple Programmable Logic Device) Implementation:

Construct an Odd Parity Checker Circuit by using SPLD logic. Odd parity logic circuit is given below in **Figure-2**.

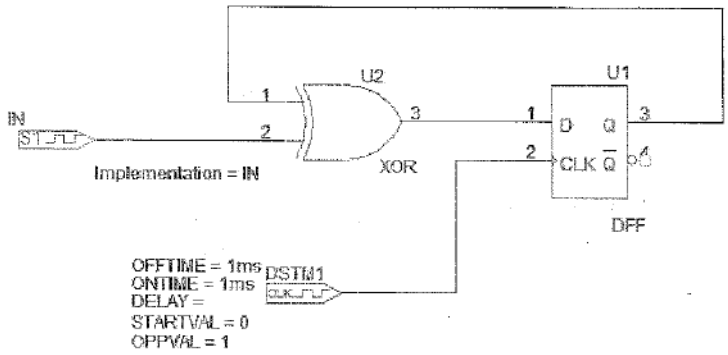


Figure-2

Construct these logic circuits by using PLA. Use "Filestim" for input,x.

References

1. http://en.wikipedia.org/wiki/Programmable_logic_array

ECE 124 LAB 11

1-) CMOS Inverter and CMOS Ex-Or Gate

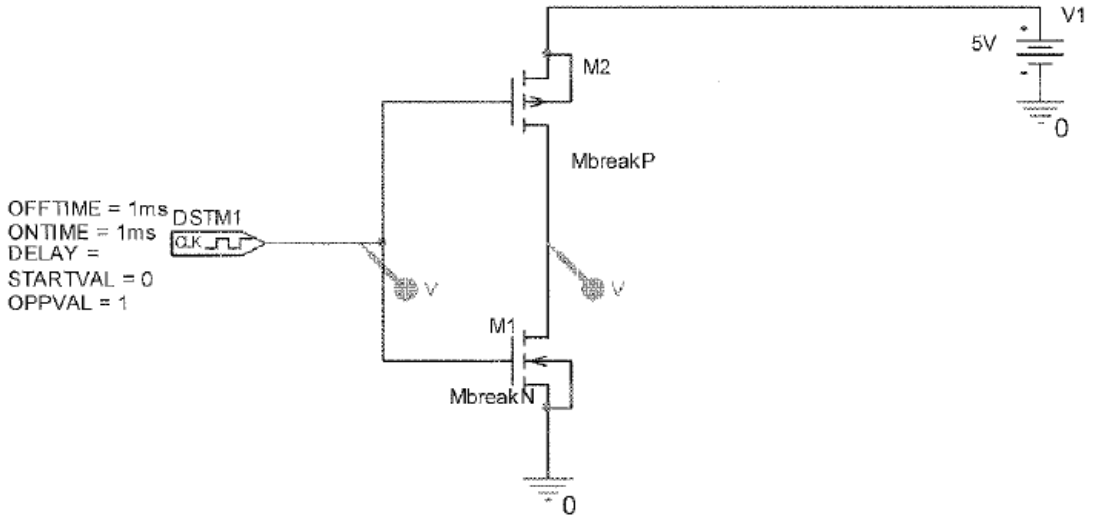
a-) Design a CMOS inverter.

b-) Design a CMOS xor gate.

Show your paper work and computer simulation circuit to your instructor.

Parts – Libraries: MBreakN,MBreakP –Breakout , VDC-Source, Digclock-Source.

NOTE: You must rote MbreakP vertically (Mirror vertically), and always connect substrates with source as shown below.



(CMOS Inverter)