# **ORCAD 9.2 CAPTURE CIS SIMULATION MANUAL**

Aim of this manual is to explain beginner users how to do simulations with logic gates. Manual consists of 4 steps and each step is explained with images.

## Step 1: Open "Capture CIS".

Open the Capture CIS program whose icon is shown in . If you can't see this icon on your desktop, search for it form "Start" menu.



Figure – 1

#### Step 2: Open a new Project.

When you open the program, **Figure-2** should be seen. As you can see from the figure a new project is opened from File -> New-> Project...



Figure – 2

When you click as shown in **Figure-2**, a new window is opened as seen in **Figure-3**. There are three important points in this window. First one is your project's name; type a meaningful name which describes your project's aim for instance "xor\_gate\_with\_nand\_gates", "2\_to\_1\_Mux". Second point is to choose your project type. In our laboratory experiments, you should always choose "Analog or Mixed A/D", otherwise you can't perform simulation. The last point is the location of your project. Create your project to your own student file for easy access.



Figure – 3

After pressing "OK" button in Figure-3. Figure-4 is opened which is named as "Create PSpice Project". You should choose "Create a blank project" then press "OK".



Figure – 4

A new project is opened. Program window should be like Figure-5. A schematic sheet is opened.

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Figure – 5

### **Step 3: Constructing the logic circuit.**

A new project is opened named as "xor\_gate\_with\_nand\_gates". We are going to construct a logic circuit with three NAND gates and two Inverters. Duty of this circuit is performing "xor" gate function. Equation of this circuit is like this:

$$Z = ((X'Y)' (YX)')'$$
 Eq. 1

To construct the logic circuit first we need to add components to the schematic sheet. There are two ways to add components to the sheet. First one is pressing the place part button. Button is on the rightmost part of the sheet, lies perpendicular to the page, can be seen at **Figure – 6**. Second one is from the Capture Menu by pressing **Place -> Part**.

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Figure – 6

There are three main component libraries that we are going to use throughout our lab works. Name of these libraries are DIG\_PRIM, SOURCE, SOURCSTM. In DIG\_PRIM, components like and gate, or gate, nand gate, xor gate, flip\_flops, multiplexers are exists. In the SOURCE library, source part of our logic circuits like DigClock,VDC are found. These elements have paramount importance for logic circuit operation; can be thought as power source. The last library is SOURCSTM; we are going to use this library as logic input of our circuits.

Now after introducing the libraries, we are going to add our first element to the circuit. Press place button shown as **Figure -6** and a window like in **Figure - 7** is opened.

Place Part			X
Part:		-	OK
Part List:			Cancel
JKFFSH NAN10 NAN11 NAN12 NAN13		^	Add Library Remove Library Part Search
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Figure – 7

Choose DIG\_PRIM library and type "NAN2" to the search part then press "OK". Place three NAND gates then to be able to stop placing this component press "ESC" button from the keyboard, **Figure-8**.





We need two inverters. Add inverter to the project by typing "INV" to the search part in **Figure - 9**.



Figure – 9

We place two inverters. Now we need to wire these logic gates to be able simulate the "xor" function. To draw wire lines choose second icon from the rightmost menu as shown in **Figure-10**. Then start wiring as shown, be careful while wiring pin to pin. To make sure they are connected see red dot like in **Figure-10**.



When you wire the circuit, next step is adding logic inputs x and y to the system. We are going to use two clock signals, which gives us "00", "01", "10", "11" conditions. These conditions are needed to be able to check whether result of "xor" gate function is true or not. To add clock signals to the system, place DigClock from the "SOURCE" library. As a result, circuit at **Figure-11** should be observed. Change OFFTIME and ONTIME values as shown in figure.



Figure - 11

These clock signals are going to be our input signals of "xor" gate. We can directly connect them to the corresponding places. However, we are going to show a new simple method. By using this method, we simplify the scene of our circuitry. For more complex logic circuits, it will be beneficial.

Press "Place off-page connector" from the rightmost menu, also shown in Figure-12.



Figure – 12

Choose OFFPAGELEFT-L, Figure-13.



Figure – 13

Place the connector as shown in **Figure-14**. Be careful about red arrows direction. If possible use "R" in keyboard to rotate the connector. Also, as you can see from the figure that connectors are renamed. You should also rename them as shown.



Figure – 14

After this operation our circuit is ready for simulation. We implemented Eq. 1 completely.

#### **Step 4: Simulation**

Simulation is going to be performed from PSpice. To make simulation, firstly we need to open a new simulation profile. Open it, as seen from **Figure-15**.



Figure-15

A new window will open. Name your simulation. In this manual, it is named as "xor\_sim", **Figure-16.** 

New Simulation	×
Name:	Create
xor_sim	Cancel
Inherit From:	
Root Schematic: SCHEMATIC1	

Figure-16

When you press "Create" button a new window is going to be opened, **Figure-17**. Type "Run to time" to 4ms. This value shows us simulation total time. 4ms is sufficient for this experiment. Click "OK" button.

Analysis type: Time Domain (Transient)   Options:  Contract Carlo/Worst Care Parametric Sweep Carlow Rise Roint Coad Bias Point	mulation Settings - xor_sim General Analysis Include File	es   Libraries   Stimulus   Options   Data Collection   Probe Window
	Analysis type: Time Domain (Transient) Options: General Settings Granetic Sweep Farametic Sweep Save Bias Point Load Bias Point	Run to time:     4mil     seconds (TSTOP)       Start saving data after:     0     seconds       Transient options     Maximum step size:     seconds       Maximum step size:     seconds     seconds       Skip the initial transient bias point calculation (SKIPBP)     Output File Options

Figure-17

Now, probes should be placed to observation locations. In this example, we want to see two inputs of the system and one output. Probes can be added from the top menu shown in **Figure-18**.



Figure-18

Now, simulation is ready. Press "Run PSpice" button from the top menu, **Figure-19**. A new window is going to be open with corresponding signals.





Observation of Figure-20 shows us that we have achieved the function of "xor" gate.



In the simulation window, for better observation you can use cursor property. Cursor can be opened like in **Figure-21**.



Figure-21

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